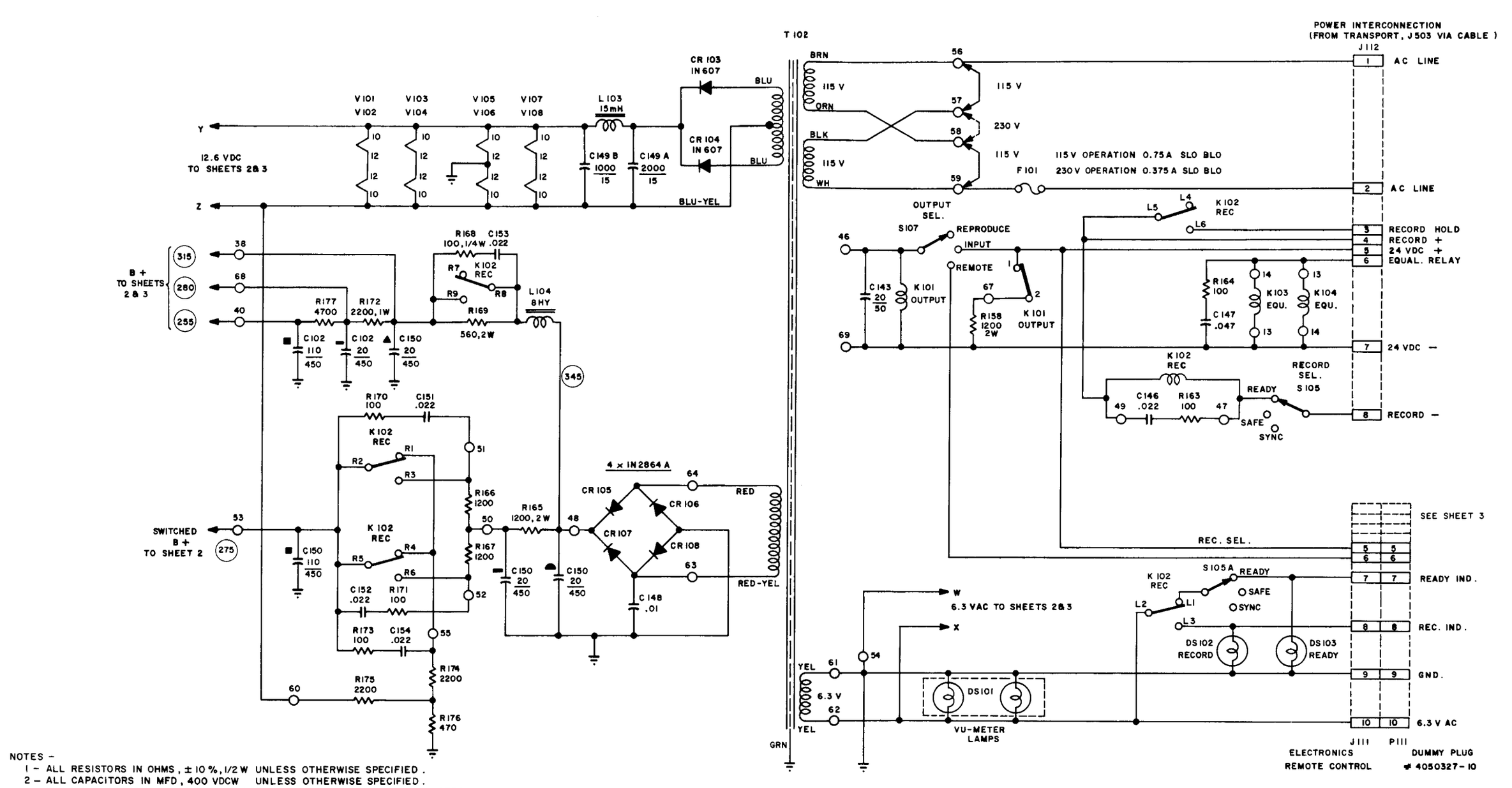


NOTES –

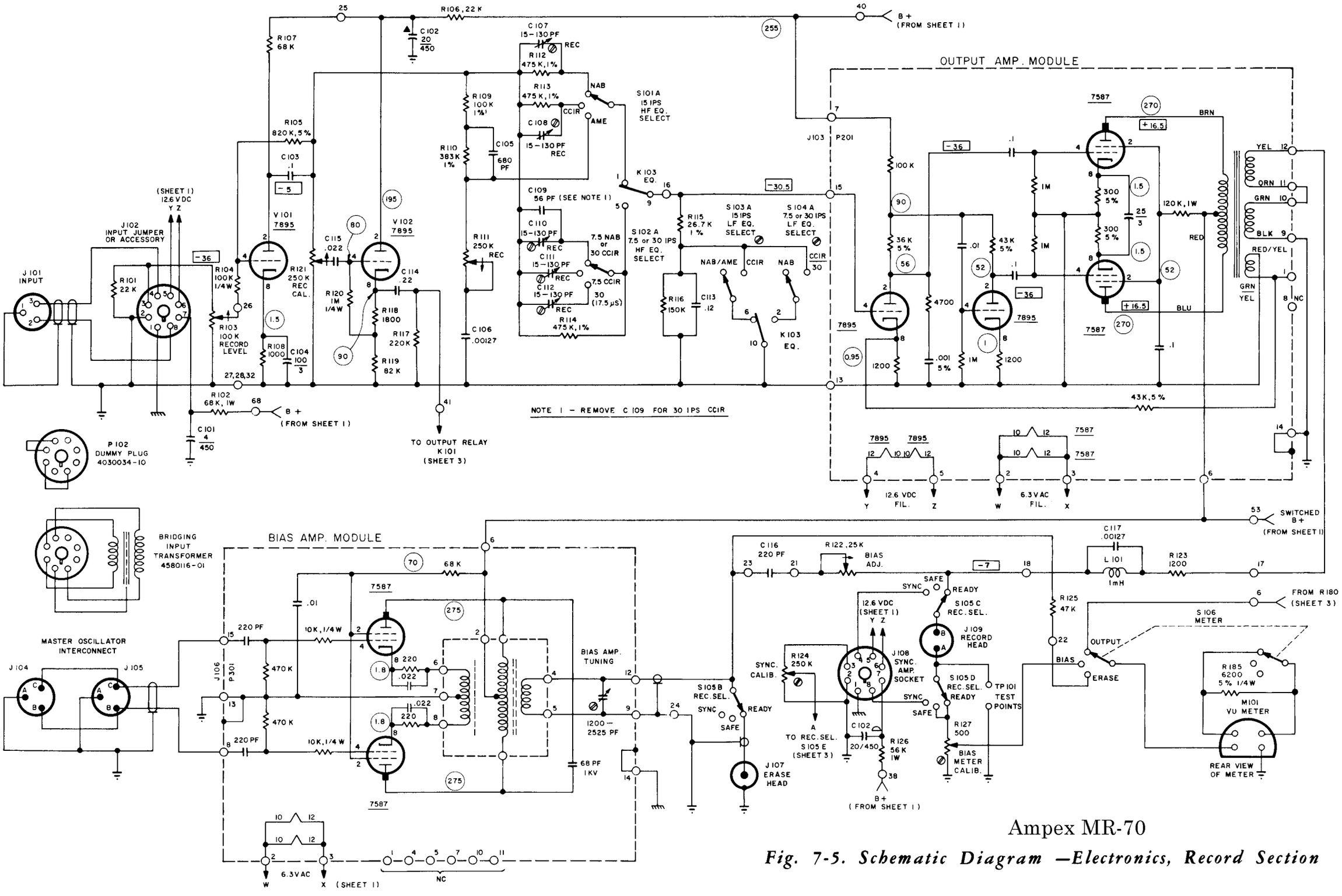
1 – ALL RESISTORS IN OHMS, ± 10 %, 1/2 W UNLESS OTHERWISE SPECIFIED.
2 – ALL CAPACITORS IN MFD, 400 VDCW UNLESS OTHERWISE SPECIFIED.
3 – SWITCHES ARE SHOWN AS THEY FUNCTION NOT AS THEY ARE CONSTRUCTED.
4 – DC VOLTAGES MEASURED FROM POINT TO GROUND USING A VTVM HAVING 10 MEG OHM INPUT RESISTANCE.
5 – SIGNAL VOLTAGES MEASURED WITH AC VTVM.

CIRCUIT CONDITIONS –

1 – REPRODUCE & ERASE HEADS DISCONNECTED – 220 OHM RESISTOR CONNECTED ACROSS TERMINALS A & B OF J 109 IN PLACE OF RECORD HEAD.
2 – BIAS OSCILLATOR INPUT DISCONNECTED.
3 – 500 CPS INPUT.
4 – REPRODUCE LEVEL CONTROL SET SO, THAT 0 DB AT TP 102 PRODUCES +8 DBM OUTPUT.
5 – RECORD LEVEL CONTROL SET FULLY CLOCKWISE.
6 – EQUALIZATION — 15 IPS NAB.
7 – ELECTRONICS IN RECORD MODE.

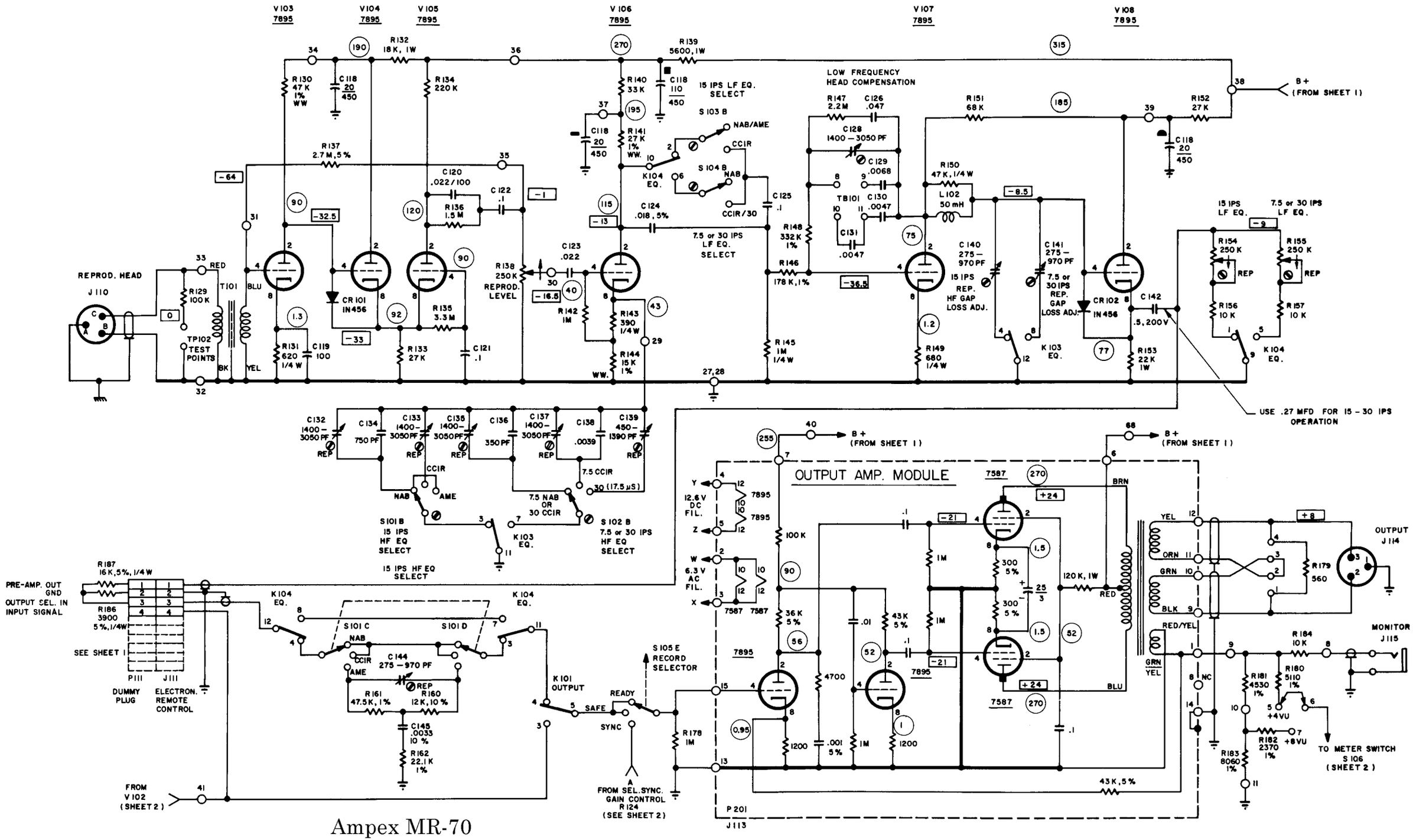
Ampex MR-70

Fig. 7-4. Schematic Diagram—Electronics, Power Supply



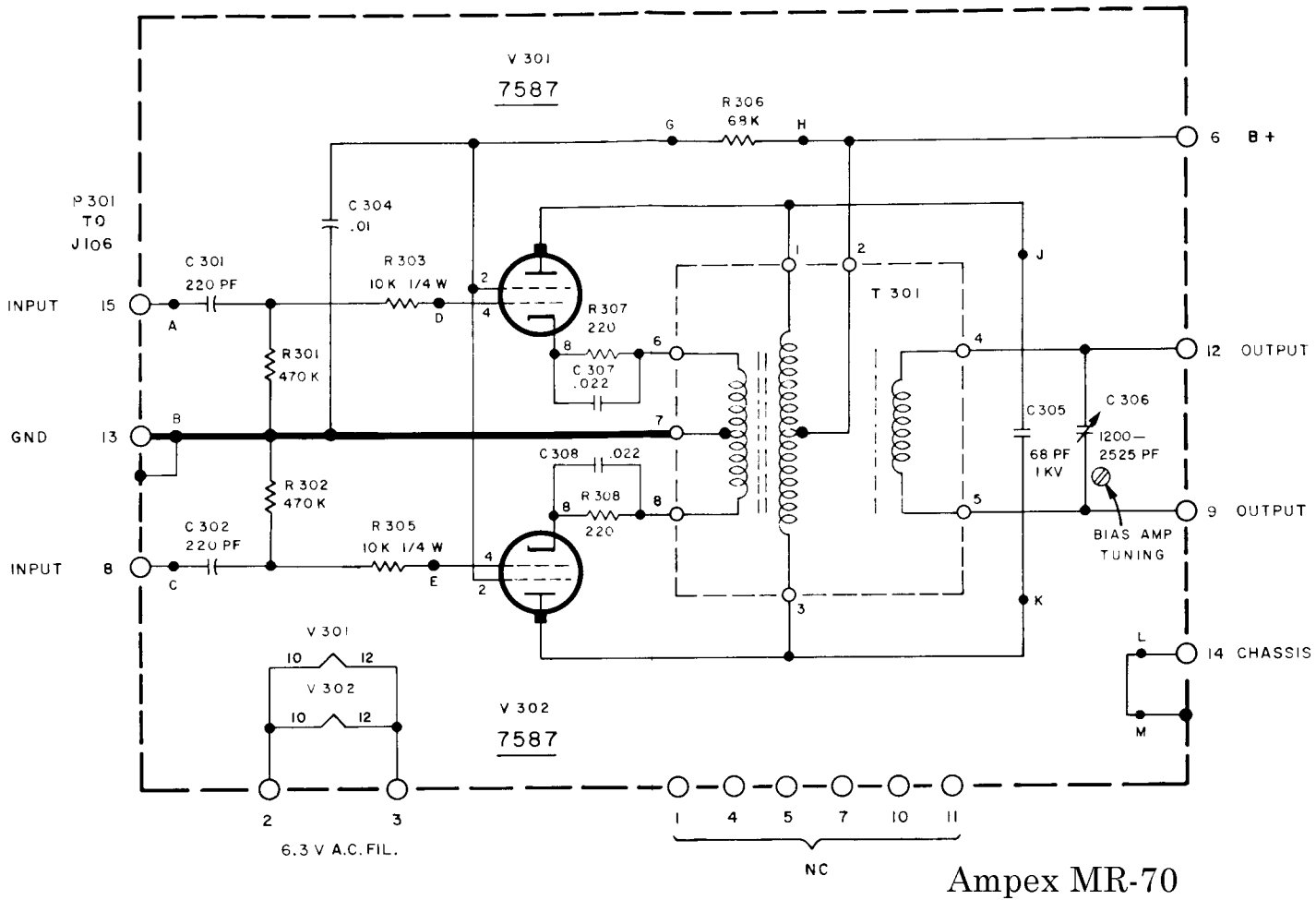
Ampex MR-70

Fig. 7-5. Schematic Diagram —Electronics, Record Section



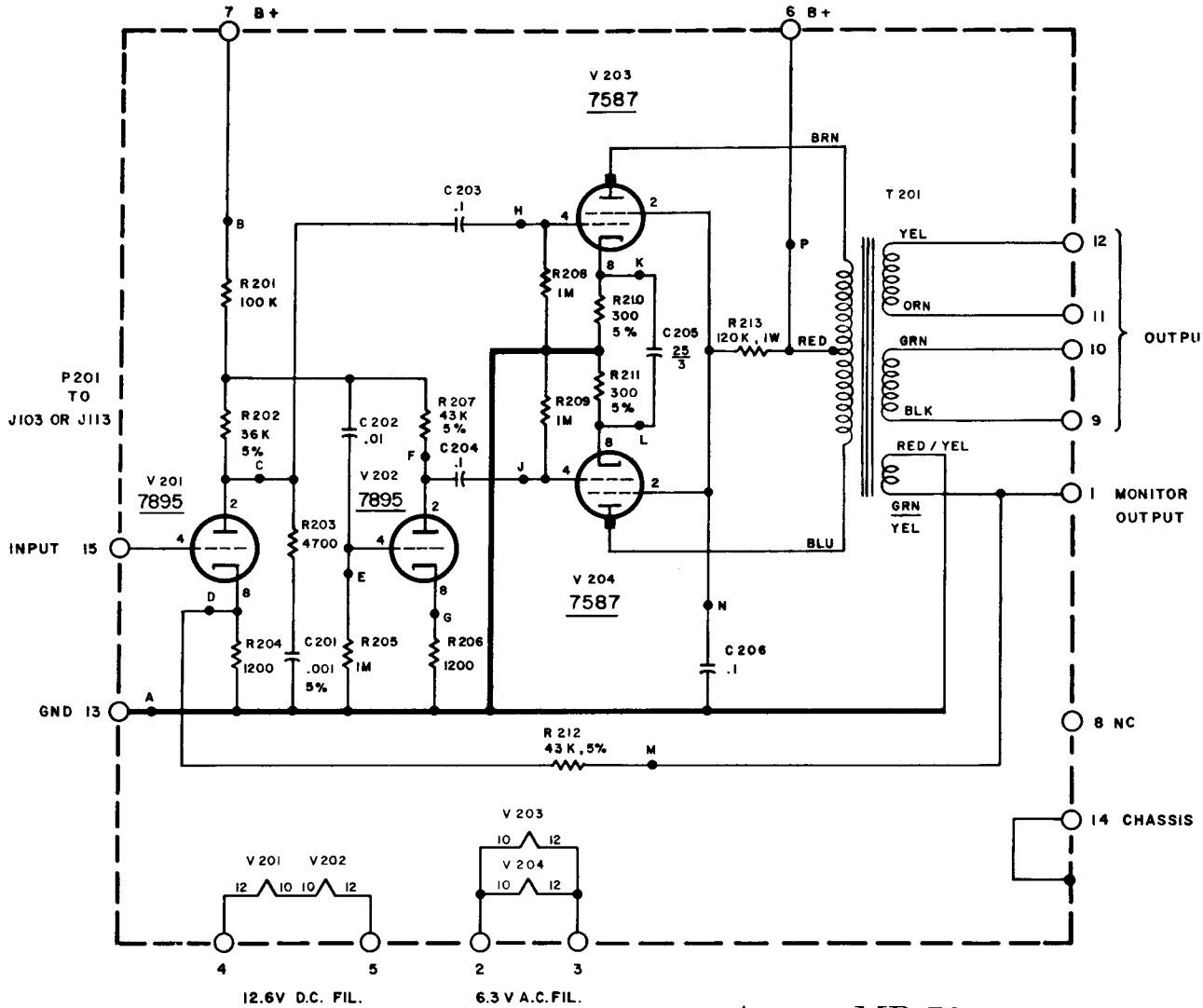
Ampex MR-70

Fig. 7-6. Schematic Diagram—Electronics, Reproduce Section



Ampex MR-70

Fig. 7-8. Schematic Diagram—Bias Amplifier Module



Ampex MR-70

Fig. 7-9. Schematic Diagram—Output Amplifier Module